LISTING OF THE CLAIMS

1. - 8. Canceled

9. (Currently Amended) A power MOSFET having reduced on resistance comprising~~, in combination,~~:

a P type conductivity substrate; an epitaxially deposited N type conductivity layer deposited atop said P type substrate to form an epitaxial layer having a substantially ~~constant~~ uniform concentration of P-type dopants throughout its volume; a plurality of spaced trenches having vertical walls extending through said epitaxial layer; a thin gate oxide on said vertical walls and conductive polysilicon with a P type conductivity deposited into said trenches to define a polysilicon gate; a P type concentration source region formed adjacent the walls of each of said trenches and diffused into the top of said epitaxial layer; a source contact connected to at least said source regions; and a drain contact made of metal and connected to a bottom surface of said substrate, wherein the doping of said N-type layer allows voltage to be blocked therein.

10. (Previously Presented) The MOSFET of claim 9, further comprising a plurality of spaced notches extending through said source regions and exposing said epitaxial deposited layer, wherein said source contact extends through said plurality of notches and is connected to said epitaxially deposited layer.

11. (Currently Amended) The MOSFET of claim 10, wherein said epitaxial layer has a resistivity of about 0.17 ohm cm and a thickness of about 2.5 μm.

12. (Currently Amended) The MOSFET of claim 9, wherein said substrate is a P^+ substrate having a resistivity of less than about 0.005 ohm cm.

13. (Currently Amended) The MOSFET of claim 10, wherein said substrate is a P^+ substrate having a resistivity of less than about 0.005 ohm cm.

14. - 22. (Canceled).